VLSI IMPLEMENTATION OF A SINGLE-CYCLE PROCESSOR FOR A SUBSET OF THE MIPS ARCHITECTURE IN VERILOG HDL(HARDWARE DESCRIPTION LANGUAGE)

ABSTRACT:

This Projects aims at HDL development/Implementation of a MIPS Processor, which supports MIPS Instruction Sub Set, which covers R-Type, I-type and J type Instruction.

The architecture of MIPS is thoroughly studies and analyzed.

Each Block is coded in Verilog HDL, and then verified. In a similar manner all the blocks of the MIPS system are coded and tested. After this stage all the blocks are integrated to form the MIPS Data Path and Instruction path.

We can write a Program, convert it to Opcode, store the Opcode in memory and execute the code and to verify if the Program is working as expected.

Once Verilog HDL code is complete, Simulations and synthesis will be done.

Following are tools which will be used

Tools: Xilinx ISE, Model Sim, Active HDL

Language: Verilog HDL